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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,310	06/27/2001	Masahito Suzuki	108066-00037	1647

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,310	SUZUKI, MASAHITO	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-10 are presented for examination.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.1 14, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.1 14, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.1 14. Applicant's submission filed on 05/11/2005 has been entered.

Response to Amendment

Applicant's arguments filed May 11, 2005 have been fully considered but they are not persuasive. The examiner attempted to contact applicant on June 6, 2005 to discuss the issues with the claim language, however there has been no response to the message left by the examiner.

Although applicant has attempted to clear up the claim language and the 35 U.S.C. 112, second paragraph issues, these attempts to clarify the claimed subject matter are insufficient. Therefore, based on the following 35 U.S.C. 112, second paragraph issues, applicant's arguments are not persuasive.

The examiner will therefore maintain the previous 35 U.S.C. 103 rejections as recited in the previous action.

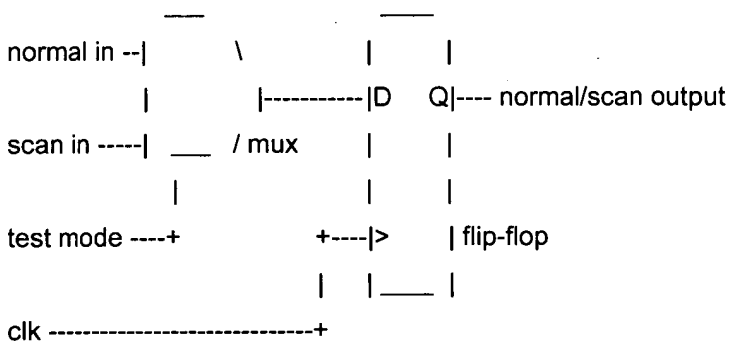
As per the amendments to the independent claims, the examiner does not see the required clarification of the claims by the amendments. The amendments fail to clear up the issues that were initially questioned. Therefore, in response to this amendment, the examiner will attempt to be more specific about the points that are unclear in the claims.

The addition of the following limitation;

"...a plurality of boundary scan registers, serially connected to constitute a shift register, for inputting and outputting scan-in data or scan-out data, the scan-in data being input to the shift register and the scan-out data being output from the shift register,"(Claim 1 lines 6-8, Claim 5 lines 8-10, Claim 9 lines 8-10)

The definition of 'scan register' per computer dictionary online is listed below:

Scan register: (circuit design) A digital logic circuit which can act either as a flip-flop or as a serial shift register and which is used to form a scan path. The most common design is a multiplexed flip-flop:



The addition of a multiplexor (mux) to each flip-flop's input allows operation in either normal or test mode. The output of each flip-flop goes to the normal functional logic as

well as to the scan input of the next multiplexor in the scan path. The other common design is level-sensitive scan design (LSSD). (1995-02-14)

The examiner fails to see that this (above) limitation adds any novelty to the independent claims.

The additional modification to the independent claims:

"...wherein each of the boundary scan registers selectively input an input data including one of an output of the input buffer and the scan-in or scan-out data, holds the input data, and selectively output either the input data or an output from one of the serial to parallel conversion circuits." (Claim 1 lines 12-15, Claim 5 lines 13-16, and Claim 9 lines14-17)

This statement has the same lack of clarity objected to previously. (Claim 1 lines 12-15, Claim 5 lines 13-16, and Claim 9 lines14-17) contain a plurality of elements or steps, which are not separated by a line indent. Line indents aid in understanding the logical grouping of a claim's elements. The following is a quotation of 37 CFR § 1.75(i):

> (i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

In response to examiners 35 U.S.C. 112, second paragraph rejection of the independent claims, applicant states: "*The claims have been amended responsive to the rejection. Furthermore, Applicant highlights Figures 4 and 8 of the drawings along with pages 12-14 and 19-20 of the Specification. It is submitted that at least the above highlighted sections of the present application clearly discloses the subject matter of the present invention, and therefore the subject matter recited in claims is definite. Hence, Applicant respectfully requests withdrawal of the rejection.*" (Page 7 lines 14-19)

The examiner would like to point out that the specification pages 12-14 and 19-20 include considerable more explanation and detail (along with figures 4 and 8) as to how the applicants' device is connected and how the device functions. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Objections

Claim 4 is objected to because of the following informalities: In line 3, "...one of the input buffer receives..." should read "...one of the input buffers receives...". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 5, and 9, "...wherein each of the boundary scan registers selectively input an input data including one of an output of the input buffer and the scan-in or scan-out data, holds the input data, and selectively output either the input

data or an output from one of the serial to parallel conversion circuits." (Claim 1 lines 12-15)

This portion of the independent claims is unclear for the following reasons:

It is unclear to the examiner how the conversion circuit takes a serial output from the input buffer (or input terminals), converts the signal to parallel, and how it loads the parallel data (as converted) to the serial boundary scan registers? (Although the specification states the BSR and the serial parallel conversion circuit 24B are provided in parallel with respect to the output of the input buffer, and that the system input is buffered with a differential input buffer, but the TID input is not) this is not in the claim language.

It is unclear to the examiner (based on the claim language) how the serially connected boundary scan registers are connected to the parallel output of the serial parallel conversion circuit (i.e. do each of the parallel outputs connect to a separate boundary scan register, or how does the parallel output load into the serial boundary scan register selectively? Here the examiner is attempting to point out that the claim language is failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. By not stating, these are separate paths, which are in parallel, as stated in the specification, and by not separating the elements – see below – the claim is indefinite. The specification seems to show that the two paths are completely independent, however the claim language in unclear on that issue).

Claims 1, 5, and 9, (lines 12-15) contain a plurality of elements or steps, which are not separated by a line indent. Line indents aid in understanding the logical grouping of a claim's elements. The following is a quotation of 37 CFR § 1.75(i):

> (i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

The dependent claims 2-4 inherit the 35 U.S.C. 112, second paragraph issues of the independent claims 1.

The dependent claims 6-8 inherit the 35 U.S.C. 112, second paragraph issues of the independent claim 5.

The dependent claim 10 inherits the 35 U.S.C. 112, second paragraph issues of the independent claim 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-6, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhong et al. U.S. Patent No. 6,014,763 in view of Whetsel U.S. Patent No. 6,405,335.

As per claims 1, 5, and 9, Dhong et al. substantially teach the claimed integrated circuit that can be tested by using the steps of transmitting a scan input in parallel from

a tester to the integrated circuit, converting the scan input at the integrated circuit from parallel to serial, and passing the serial scan input through scan circuitry of the integrated circuit, to create a serial scan output. This circuit provides for transmitting a scan data input in parallel, and transmitting a scan enable input in parallel. If loading the caches through the scan chain is desired, the control signal (cache enable) is also transmitted in parallel. The scan output can further be converted from serial to parallel, and the scan output transmitted in parallel from the integrated circuit to the tester. The scan enable input can be distributed to the scan circuitry using a plurality of multiplexers configured in a tree structure. (Column 3 lines 7-33) Not disclosed in Dhong et al. is the use of input buffers.

However, in an analogous art, Whetsel teaches an integrated circuit for testing in which the input signal is input to a series of input buffers connected to the individual scan paths (column 28, lines 45-61). Whetsel also teaches that when the integrated circuit's functional circuitry is configured for testing, all functional registers (flip/flops or latches) in the integrated circuit are converted into scan registers that form the parallel scan paths shown. Also, during test configuration, all combinational logic in the integrated circuit that was associated with the functional registers remains associated with the scan registers after the conversion. This conversion of an integrated circuit's functional circuitry into scan paths and combinational logic is well known. (Column 5 lines 40-49) Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the input buffer circuitry of Whetsel in conjunction with the scan path testing taught by Dhong et al. This would

have been obvious as suggested by Whetsel (column 20, lines 32-37 column 28, lines 36-44) in order to separate the signals to each path and to reduce the power consumption, and to allow them to drive (at the required speed) the internal circuits to which they are connected during a scan sequence.

As per claims 2, 3, 6, and 8, Dhong et al. teach that the scan enable input can be distributed to the scan circuitry using a plurality of multiplexers (selectors) configured in a tree structure. As further illustrated in FIG. 5, the scan chain is preferably implemented using additional multiplexer input ports to reduce the load on each distributed signal. The scan enable line is fed to multiple inputs of another multiplexer/latch, which splits the signal into different lines that are fed to second-level multiplexer/latches. The outputs of each of the second-level multiplexer/latches can be similarly split to provide another four inputs to four third-level multiplexer/latches. In this manner, 48 identical scan enable outputs can be provided (output selectors). This tree structure for distributing the scan chain can allow the scan speed to actually exceed the processor's normal operational speed. In a similar manner, another multiplexer/latch can be used as illustrated in FIG. 6, to divide the cache enable signal into two identical signals, one for the instruction cache, and one for the data cache. (Column 5 lines 46-62 and Fig 5 and Fig 6)

Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhong et al. U.S. Patent No. 6,014,763 in view of Whetsel U.S. Patent No. 6,405,335as applied to claims 1-3, 5-6, and 8-10 above, and further in view of Lai et al. U.S. Patent No. 6,763,486.

As per claims 4 and 7, Dhong et al. and Whetsel as applied to claims 1-3, 5-6, and 8-10 above, substantially teach the claimed integrated circuit device in which the claimed integrated circuit can be tested by using the steps of transmitting a scan input in parallel from a tester to the integrated circuit, converting the scan input at the integrated circuit from parallel to serial, and passing the serial scan input through scan circuitry of the integrated circuit, to create a serial scan output. This circuit provides for transmitting a scan data input in parallel, and transmitting a scan enable input in parallel. If loading the caches through the scan chain is desired, the control signal (cache enable) is also transmitted in parallel. The scan output can further be converted from serial to parallel, and the scan output transmitted in parallel from the integrated circuit to the tester. The scan enable input can be distributed to the scan circuitry using a plurality of multiplexers configured in a tree structure. (Dhong et al. Column 3 lines 7-33) And further, Whetsel teaches an integrated circuit for testing in which the input signal is input to a series of input buffers connected to the individual scan paths (column 28, lines 45-61). Whetsel also teaches that when the integrated circuit's functional circuitry is configured for testing, all functional registers (flip/flops or latches) in the integrated circuit are converted into scan registers that form the parallel scan paths shown. Also, during test configuration, all combinational logic in the integrated circuit that was associated with the functional registers remains associated with the scan registers after the conversion. This conversion of an integrated circuit's functional circuitry into scan paths and combinational logic is well known. (Whetsel Column 5 lines 40-49)

Not disclosed by the above combination is that the integrated circuit device input and outputs include differential inputs and outputs to the input and output buffers.

However, in an analogous art, Lai et al. teach a method for boundary scan testing that uses differential inputs to the input buffer and differential outputs (Abstract, column 1 lines 52-60 column 5 lines 1-42 Figures 6 and 7, claims 1 and 12). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the differential inputs and outputs of Lai et al. with the integrated circuit device of Dhong et al. and Whetsel as combined above, This combination would have been obvious in order to detect the common defects which are masked by the AC coupling on high speed signal paths (Lai et al. column 1 lines 26-38).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133